Low-Voltage CMOS Octal Transparent Latch

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX373 is a high performance, non-inverting octal transparent latch operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_{\rm I}$ specification of 5.5 V allows MC74LCX373 inputs to be safely driven from 5 V devices.

The MC74LCX373 contains 8 D-type latches with 3-state outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are enabled. When \overline{OE} is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0 \text{ V}$
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in all Three Logic States (10 μA)
 Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA

• ESD Performance: Human Body Model >2000 V

Machine Model >200 V

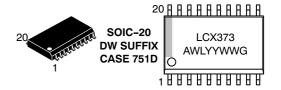
Pb-Free Packages are Available*

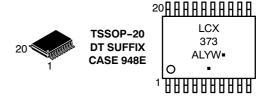


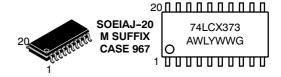
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS







A = Assembly Location

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

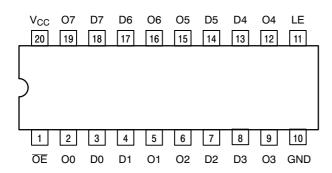


Figure 1. Pinout (Top View)

PIN NAMES

PINS	FUNCTION
ŌĒ	Output Enable Input
LE	Latch Enable Input
D0-D7	Data Inputs
00-07	3-State Latch Outputs

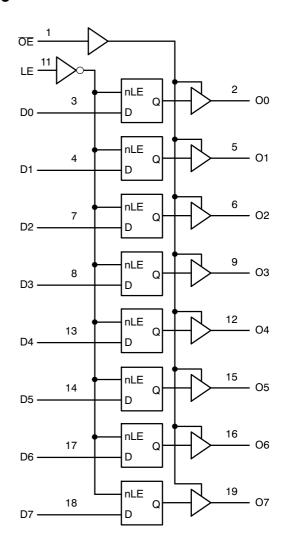


Figure 2. Logic Diagram

TRUTH TABLE

	INPUTS		OUTPUTS	
OE	LE	Dn	On	OPERATING MODE
L L	H	H L	H L	Transparent (Latch Disabled); Read Latch
L L	L L	h I	H L	Latched (Latch Enabled) Read Latch
L	L	Х	NC	Hold; Read Latch
Н	L	Х	Z	Hold; Disabled Outputs
H H	H	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	L L	h I	Z Z	Latched (Latch Enabled); Disabled Outputs

High Voltage Level

High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition h

Low Voltage Level

Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition

NC = No Change, State Prior to the Latch Enable High-to-Low Transition

X Z = High or Low Voltage Level or Transitions are Acceptable

= High Impedance State

For I_{CC} Reasons DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	$-0.5 \le V_1 \le +7.0$		V
Vo	DC Output Voltage	$-0.5 \le V_0 \le +7.0$	Output in 3-State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
lok	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
Io	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Тур	Max	Unit
V _{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
VI	Input Voltage		0		5.5	V
V _O	Output Voltage (HIGH or LOW State) (3-State)	0		V _{CC} 5.5	V
I _{OH}	HIGH Level Output Current	V _{CC} = 3.0 V - 3.6 V V _{CC} = 2.7 V - 3.0 V V _{CC} = 2.3 V - 2.7 V			- 24 - 12 - 8	mA
I _{OL}	LOW Level Output Current	V _{CC} = 3.0 V - 3.6 V V _{CC} = 2.7 V - 3.0 V V _{CC} = 2.3 V - 2.7 V			+ 24 + 12 + 8	mA
T _A	Operating Free-Air Temperature		-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8	V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V

^{1.} I_O absolute maximum rating must be observed.

DC ELECTRICAL CHARACTERISTICS

			T _A = -40°C	to +85°C	
Symbol	Characteristic	Condition	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		1
V_{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	1
V _{OH}	HIGH Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ I}_{OL} = 100 \mu\text{A}$	V _{CC} - 0.2		V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8		1
		$V_{CC} = 2.7 \text{ V}; I_{OH} = -12 \text{ mA}$	2.2		1
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -18 \text{ mA}$	2.4		1
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		1
V _{OL}	LOW Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ I}_{OL} = 100 \mu\text{A}$		0.2	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	1
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	1
I _I	Input Leakage Current	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_{I} \le 5.5 \text{ V}$		±5	μΑ
I _{OZ}	3-State Output Current	$2.3 \le V_{CC} \le 3.6 \text{ V}; \ 0V \le V_O \le 5.5 \text{ V};$ $V_I = V_{IH} \text{ or } V_{IL}$		±5	μΑ
I _{OFF}	Power-Off Leakage Current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$		10	μΑ
I _{CC}	Quiescent Supply Current	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_I = \text{GND or } V_{CC}$		10	μΑ
		$2.3 \le V_{CC} \le 3.6 \text{ V}; \ 3.6 \le V_{I} \text{ or } V_{O} \le 5.5 \text{ V}$		±10	1
ΔI_{CC}	Increase in I _{CC} per Input	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_{IH} = V_{CC} - 0.6 \text{ V}$		500	μΑ

^{2.} These values of V_{I} are used to test DC electrical characteristics only.

AC CHARACTERISTICS t_R = t_F = 2.5 ns; R_L = 500 Ω

					Lin	nits			
				T _A = -40°C to +85°C					
			V _{CC} = 3.3	3 V ± 0.3 V	V _{CC} =	2.7 V	V _{CC} = 2.5	V ± 0.2 V	
			C _L =	50 pF	C _L =	50 pF	C _L =	30 pF	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	1	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	1.5 1.5	9.6 9.6	ns
t _{PLH} t _{PHL}	Propagation Delay LE to O _n	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	1.5 1.5	10.5 10.5	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	1.5 1.5	10.5 10.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	1.5 1.5	9.0 9.0	ns
t _s	Setup Time, HIGH or LOW D _n to LE	3	2.5		2.5		4.0		
t _h	Hold Time, HIGH or LOW D _n to LE	3	1.5		1.5		2.0		
t _w	LE Pulse Width, HIGH	3	3.3		3.3		4.0		
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0					ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

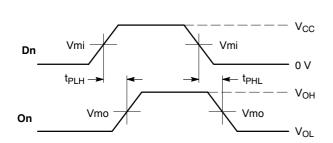
DYNAMIC SWITCHING CHARACTERISTICS

			T,	_A = +25°	С	
Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V _{OLP}	Dynamic LOW Peak Voltage (Note 4)	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V} \\ V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		0.8 0.6		V V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4)	$\begin{aligned} &V_{CC} = 3.3 \text{ V, } C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{ V, } V_{IL} = 0 \text{ V} \\ &V_{CC} = 2.5 \text{ V, } C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{ V, } V_{IL} = 0 \text{ V} \end{aligned}$		-0.8 -0.6		V V

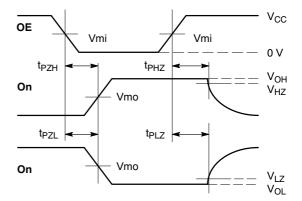
^{4.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

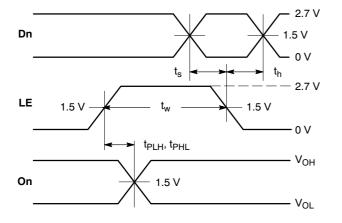
Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	7	pF
C _{I/O}	Input/Output Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	25	pF



 $\label{eq:waveform 1 - PROPAGATION DELAYS} \\ t_R = t_F = 2.5 \text{ ns}, 10\% \text{ to } 90\%; \text{f} = 1 \text{ MHz}; t_W = 500 \text{ ns}$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES $t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; f = 1 MHz; $t_W = 500 \text{ ns}$

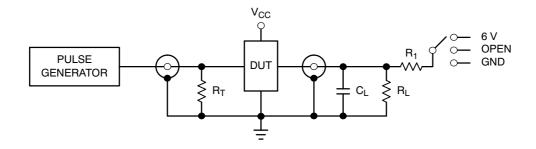


	Vcc				
Symbol	3.3 V \pm 0.3 V	2.7 V	2.5 V \pm 0.2 V		
Vmi	1.5 V	1.5 V	V _{CC} /2		
Vmo	1.5 V	1.5 V	V _{CC} /2		
V _{HZ}	V _{OL} + 0.3 V	V _{OL} + 0.3 V	V _{OL} + 0.15 V		
V_{LZ}	V _{OH} - 0.3 V	V _{OH} - 0.3 V	V _{OH} – 015 V		

WAVEFORM 3 - LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES

 t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns except when noted

Figure 3. AC Waveforms



TEST	SWITCH
t _{PLH} , t _{PHL}	Open
tpzl, tplz	6 V at V _{CC} = 3.3 ± 0.3 V 6 V at V _{CC} = 2.5 ± 0.2 V
Open Collector/Drain t _{PLH} and t _{PHL}	6 V
t _{PZH} , t _{PHZ}	GND

 C_L = 50 pF at V_{CC} = 3.3 \pm 0.3 V or equivalent (includes jig and probe capacitance) C_L = 30 pF at V_{CC} = 2.5 \pm 0.2 V or equivalent (includes jig and probe capacitance) R_L = R_1 = 500 Ω or equivalent

 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

ORDERING INFORMATION

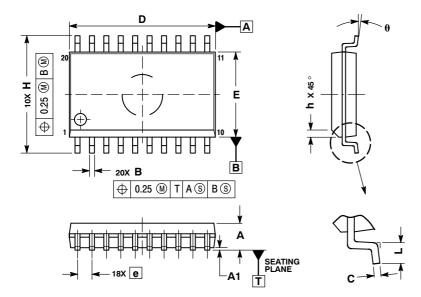
Device	Package	Shipping [†]
MC74LCX373DWR2	SOIC-20	1000 Tape & Reel
MC74LCX373DWR2G	SOIC-20 (Pb-Free)	1000 Tape & Reel
MC74LCX373DT	TSSOP-20*	75 Units / Rail
MC74LCX373DTG	TSSOP-20* (Pb-Free)	75 Units / Rail
MC74LCX373DTR2	TSSOP-20*	2500 Tape & Reel
MC74LCX373DTR2G	TSSOP-20* (Pb-Free)	2500 Tape & Reel
MC74LCX373MEL	SOEIAJ-20	2000 Tape & Reel
MC74LCX373MELG	SOEIAJ-20 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}This package is inherently Pb-Free.

PACKAGE DIMENSIONS

SOIC-20 **DW SUFFIX** CASE 751D-05 ISSUE G

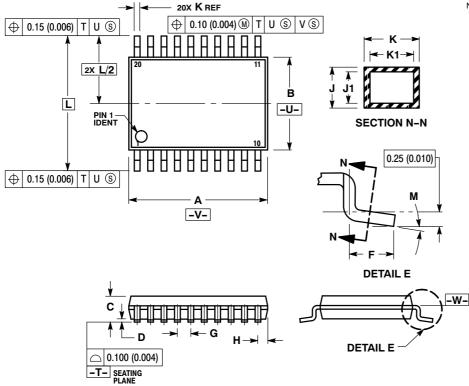


- NOTES:
 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS				
DIM	MIN	MAX			
Α	2.35	2.65			
A1	0.10	0.25			
В	0.35	0.49			
С	0.23	0.32			
D	12.65	12.95			
Е	7.40	7.60			
е	1.27	BSC			
Н	10.05	10.55			
h	0.25	0.75			
L	0.50	0.90			
A	0 °	7 °			

PACKAGE DIMENSIONS

TSSOP-20 **DT SUFFIX** CASE 948E-02 ISSUE C



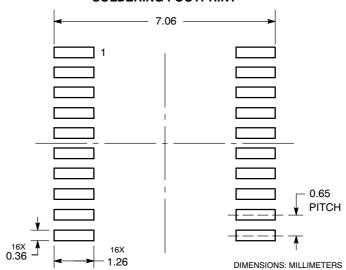
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER
 - SIDE. SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 - CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

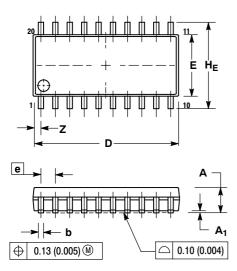
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	6.40	6.60	0.252	0.260
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

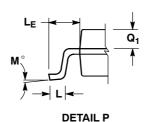
SOLDERING FOOTPRINT

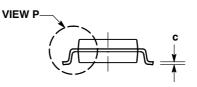


PACKAGE DIMENSIONS

SOEIAJ-20 **M SUFFIX** CASE 967-01 **ISSUE A**







NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- B. DIMENSIONS D AND E DO NOT INCLUDE
 MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
- 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE
 BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
Е	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q ₁	0.70	0.90	0.028	0.035
Z		0.81		0.032

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice on semiconductor and are registered raderians of semiconductor Components industries, Ite (SciLLC) solicit esserves the right to make changes without further holice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA **Phone**: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative